Remarks

Claims 1-20 are pending in this application. The examiner has rejected claims 1, 2 and 4-6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Publication No. 2003/0046464 to Murty et al. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. Further, claims 7-15, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of U.S. Patent No. 6,857,084 to Giles.

A. Claims rejected under 35 U.S.C. 102

Claims 1, 2, 4, 5, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Murty et al. (U.S. Publication Number 2003/0046464). Because the Examiner rejected independent claim 1 under section 102(b) on the basis of Murty, each element of the claim must be disclosed in Murty. Murty, however, does not disclose each element of independent claim 1. Specifically, Murty does not disclose the claimed element of each of the processors being serially released from the interrupt mode so as to reduce contention by the processors for system resources upon release from the interrupt mode.

In accordance with the present invention, the processors exit from the interrupt mode on a serial basis according to a time delay managed by the interrupt handling processor. (Summary, page 4, lines 16-18). Following the completion of processing task necessary to clear the system management interrupt, the interrupt handling processor selects one of the non-interrupt handling processors and releases that processor from the interrupt mode by setting its presence bit to a logical NO. (Detailed Description, page 9, lines 10-13). After selecting a first non-interrupt handling processor and releasing it from the interrupt mode, the interrupt handling processor pauses for a predetermined period sufficient to allow the selected processor the

opportunity to retreive its register contents from its associated SMRAM location. (Detailed Description, page 9, lines 22-25). Once the predetermined period has lapsed, the interrupt handling processor determines whether all the non-interrupt handling processors have been released from the interrupt mode. (Detailed Description, Page 10, lines 1-3). If not, then the interrupt handling processor will select the next non-interrupt handling processor and carry out the same steps. (Detailed Description, Page 10, lines 3-5). Accordingly, claim 1 discloses an information handling system where the interrupt handling processor releases the non-interrupt handling processors serially from the interrupt handling mode thereby reducing the contention by the processors for resources of the computer system including the processor bus and memory.

On the other hand, Murty discloses a multi processor system wherein the first logical processor to access the shared register handles the common interrupt and the non-interrupt handling processors return from the interrupt. (Murty, Abstract; paragraphs [0032], [0037], [0049]). Murty is completely silent on serially releasing the non-interrupt handling processors from the interrupt mode.

Because Murty fails to disclose serially releasing the non-interrupt handling processors from the interrupt mode as disclosed in independent claim 1, it fails to support a finding of anticipation under 35 U.S.C. 102(b) and the Applicant requests that this rejection be withdrawn. Claims 2-6 depend directly or inderectly from independent claim 1 and are therefore allowable for at least the same reason.

B. Claims rejected under 35 U.S.C. 103

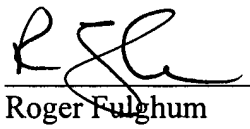
Claims 7-15, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles (U.S. Patent No. 6,857,084). Independent claims 7 and 17 recite a method for exiting from an interrupt mode in a multiple processor computer system

comprising initiating on serial basis the exit of each processor from the interrupt mode. As discussed above, Murty fails to disclose the serial release of non-interrupt handling processors from the interrupt mode. Because, like Murty, Giles fails to disclose the serial release of non-interrupt handling processors from the interupt mode, independent claims 7-17 are allowable. Claims 8-16 and 18-20 depend directly or indirectly from independent claims 7 and 17 and are therefore allowable for at least the same reasons.

Conclusion

Applicants respectfully submit that claims 1-20 should be passed to issuance.

Respectfully submitted,



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